REMARKS

Summary

Claims 30-53 and 72-101 were pending. Claims 83-100 have been cancelled, Claim 52 amended, and Claims 102-119 added. No new matter has been added as a result of this amendment. Claims 30-53, 72-82, and 101-119 are pending after entry of this amendment.

Interview Summary

Applicants thank the Examiner for the personal interview on August 10, 2005 with Applicants' Agent Anthony P. Curtis, Ph.D. (Reg. 46,193). During the interview, Applicants' Agent and the Examiner discussed the terms in Claim 30 and the dependent claims as well as the election requirement. More specifically, Applicants' Agent and the Examiner discussed the definition of a "low temperature grown semiconductor" as well as discussing various other distinctions between the bonding layers and structures of the claims in the instant application and the cited reference.

Restriction/Election

During the personal interview, the Examiner indicated that newly added Claims 72-77 and 81 are withdrawn from consideration as they are directed to a different species, which were not part of the original restriction requirement of January 26, 2005.

Regarding Claims 72-77: although the Examiner indicated that all of Claims 72-77 are withdrawn, Applicants submit that at least one of the species in Claims 72-77 should be electable at least as each of these claims recite fabrication of a particular apparatus while none of the previously presented claims (Claims 30-53) recite a similar fabrication. Applicants thus elect, with traverse, the species directed towards Claim 73, in which the bonding method is used to fabricate a transistor. Applicants further note that as Claim 30 is a generic claim, upon which all of Claims 72-77 rely, should Claim 30 be allowable, all of the withdrawn claims should be allowable.

Regarding Claim 81: Claim 81 recites a method of bonding two structures in which at least one of the structures on which the low temperature grown semiconductor is provided is specified. While during the interview the Examiner indicated that a multiple quantum well structure is a device similar to Claims 72-77, Applicants traverse this. Applicants submit that 1) unlike Claims 72-77, which recite further fabrication of the bonded structure, Claim 81 recites a structure on which the bonding takes place. This is similar to Claims 78-80, which also recite at least one of the structures on which the low temperature grown semiconductor is provided. Whether these claims recite that the underlying structure comprises a semi-insulating substrate (Claim 78), an insulator (Claim 79), a pseudomorphic structure (Claim 80), or a multiple quantum well structure (Claim 81), this is different from further fabrication of the bonded structure. 2) The Examiner indicated that a multiple quantum well structure is a device, similar to Claims 72-77. However, a multiple quantum well structure can be used in devices such as photodetectors or photoemitters, but is not a device in and of itself. Accordingly, Applicants traverse the withdrawal of Claim 81.

Objection to Claims

Claims 83-101 were objected to under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim. More specifically, the Examiner indicated that the scope of Claims 83-101 were no different from the scope of Claims 30-53.

Claims 83-100 have been cancelled. This cancellation is to expedite prosecution only.

Independent Claim 101 recites depositing Ga-rich low temperature grown compound semiconductor bonding layers. Nowhere does Claim 30 recite that the low temperature grown semiconductor bonding layers are Ga-rich. Accordingly, Applicants traverse the objection.

Furthermore, Claims 30-35, 43, 86-88 and 92 were objected to for informalities. Specifically, the Examiner objected to the phrase "the bonding layer comprises at least one of amorphous and polycrystalline [(Ga,As), (Ga,P), or (Ga,N)]" in Claims 33-35 as

being vague and ambiguous because "[d]oes (Ga,As) or (Ga,P), or (Ga,N) modify amorphous or polycrystalline?" Applicants traverse the objection as it is clear that each of amorphous or polycrystalline modify the materials (Ga,As), (Ga,P), or (Ga,N). Thus, the bonding layer recited respectively in the claims comprises amorphous (Ga,As) or (Ga,P), or (Ga,N) and/or polycrystalline (Ga,As), (Ga,P), or (Ga,N). The claims would make no sense with any other recitation, at least as a semiconductor cannot comprise "amorphous" or "polycrystalline" alone without any further modifier, such as some type of material.

Although no grounds have been laid out for the objection to Claims 30-32 or 43 (the rejections of Claims 86-88 and 92 have been rendered moot by the cancellation of the claims), Applicants assume that the objection to Claims 30-32 were the result of a typographical error (the Examiner meant to type Claims 33-35, which are similar in scope to Claims 86-88). Further, Applicants assume that the Examiner objected to the phrase "the deposition deposits at least one of low temperature grown (Ga,As), (Ga,P) and (Ga,N) on at least one of the first and second structures" in Claim 43. If this is the case, in Claim 43 it is clear that low temperature grown (Ga,As), low temperature grown (Ga,P) and/or low temperature grown (Ga,N) is deposited on the first structure and/or the second structure at least as (Ga,As), (Ga,P) and (Ga,N) are used throughout the specification to denote low temperature grown material. Accordingly, Applicants traverse the objection.

Rejection of Claims

Claims 30-53, 78-80, and 82-101 were rejected under 35 U.S.C. §102(b) as being anticipated by Malik (6,881,644). Applicants traverse the rejection.

Claim 30 recites, inter alia, depositing low temperature grown semiconductor bonding layers on first and second structures to form a combined structure. Malik does not anticipate or disclose depositing low temperature grown semiconductor bonding layers.

More specifically, the Examiner indicates that Malik discloses low temperature grown semiconductor bonding layers 52, 54 in Fig. 3D (and assumedly, portions of the specification related to that figure). Layers 52 and 54, similar to layers throughout Malik

in other embodiments, are described as porous or non-porous. However, nowhere does Malik teach the use of low temperature grown semiconductor layers in bonding the combined structure. The term porous (or non-porous) is not synonymous with the term low temperature grown.

During the interview, the Examiner asserted that the term "low temperature grown semiconductor" was relative and therefore Malik was applicable. Applicants disagree for at least two reasons: 1) the term "low temperature grown semiconductor" has particular meaning in the art, 2) even if this were not the case, there is no indication in Malik of low temperature growth conditions.

In general, semiconductors are grown at normal temperatures that produce single crystal structures, such as typical growth temperatures on the order of 500°C for MBE growth. Low temperature grown semiconductors are grown at temperatures lower than normal growth temperatures, such as about 100°C or below, as provided in the non-exclusive example of MBE growth in the specification. Other examples of temperatures for MBE and other growth techniques are readily available in the literature of this art. In some examples, low temperature growth varies up to about 100 or so degrees below that of the normal growth temperature for the various techniques. In other examples, low temperature growth provides not a single crystalline material but a polycrystalline or amorphous material. Note that polycrystalline or amorphous material can be created in ways other than low temperature growth. Applicants note that they are merely indicating examples, and that other definitions of low temperature grown semiconductors is readily available in the literature of this art. Examples of the art can be found in the previously submitted IDS (e.g., K. L. Chang, G.W. Pickrell, D.E. Wohlert, J.H. Epple, H.C. Lin, K.Y. Cheng and K.C. Hsieh, Microstructure and Wet Oxidation of Low-Temperature-Grown Amorphous (Al/Ga,As), American Institute of Physics, Vol. 89 No. 1, pgs. 747-752, January 1, 2001; G.W. Pickrell, K.L. Chang, H.C. Lin, K.C. Hsieh and K.Y. Cheng, Very-Low-Temperature Molecular Beam Epitaxial Growth of GaP/AlAs Heterostructures for Distributed Bragg Reflector Applications, American Vacuum Society; pgs. 1536-1540, July/Aug. 2001, to pick two from the IDS presented).

Moreover, only a single sentence in Malik discusses growth of the semiconductor layer (col. 11, lines 30-32). In this sentence, he states that, "[o]n the porous layer 101

thus formed, a non-porous single-crystal silicon layer 102 is epitaxially-grown (FIG. 4B)." Such a sentence, if it describes any semiconductor growth conditions at all, describes normal temperature semiconductor growth conditions, not low temperature growth conditions. Nowhere does Malik describe any growth temperature, let alone a growth temperature that would produce a low temperature grown semiconductor layer for any of the layers described therein.

The fact that Malik does not describe the growth conditions is unsurprising as Malik is directed towards a technique for improving surface texture or surface characteristics of a film for treating or smoothing a cleaved film from a layer transfer process for the manufacture of integrated circuits. That is, Malik is directed towards various embodiments to smooth or treat a surface only after the underlying structure has been cleaved (for example, the claims all require separation of the surface and then further treatment such as removal of layers and smoothing).

For at least these reasons, Malik neither anticipates nor discloses the arrangement of Claim 30. Accordingly, Claim 30 is patentable over Malik.

Dependent Claims 31-53, 78-80 and 82 are dependent upon an allowable claim. Thus, the dependent claims are allowable, without more.

However, the dependent claims are also independently patentable over Malik. For example, Claims 31 and 32 recite applying the pressure substantially uniformly to the combined structure during annealing, and that the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material, respectively. Although the Examiner points to col. 7, lines 55-65 as describing these features, neither this section nor any other actually discloses either of these features. The closest match appears to be Col. 8, lines 1-7, which describes the arbitrary selection of polycrystalline material for deposition, but is silent about formation of polycrystalline material during annealing.

Claims 33-35, 43, and 52 recite the use of bonding layers specifically formed of low temperature grown (Ga,As) or (Ga,P), or (Ga,N) or a Ga-rich layer. As discussed above, nowhere does Malik disclose using a low temperature grown semiconductor

layer as a bonding layer, let alone specifically, (Ga,As) or (Ga,P), or (Ga,N) or (Ga,N), or a Ga-rich layer.

Moreover, Claims 33-35 recite particulars regarding the annealing temperatures and times. The passages pointed to by the Examiner in col. 12 refer to heat treatment after bonding, for example for oxidation, not during bonding. In fact, these passages specifically teach away from the Claims as in col. 11, line 65 – col. 12, line 5, Malik teaches that it is necessary to choose low temperatures so that the porous layer does not change structurally (e.g. from an amorphous structure to a polycrystalline structure). In fact, the annealing temperatures are not even mentioned in Malik; only the subsequent thermal treatment temperatures are discussed.

Claim 36 recites that the bonding layers are placed in contact with each other without regard for a relative angular orientation of the first and second structures to each other. The Examiner points to Fig. 3D, however, neither Fig. 3D nor the associated text discloses angular orientation of the first and second structures. In fact, Malik is silent throughout the patent regarding the angular orientation. Similarly, Claim 42 recites that the deposition deposits between about 3 nm and about 600 nm of material on each of the first and second structures and Claims 78-80 recite specifics about the substrate and structures. The Examiner points to Fig. 3D as disclosing the thickness of the deposition as well as the other specifics recited (such as one or more of the structures containing an insulator or being psuedomorphic). However, nowhere in the Fig. 3D, nor in the text does Malik specify the thickness of the layer or other specifics about the substrate and structures recited in these claims.

Claims 39 and 41 recite that the annealing of the combined structure occurs under conditions that are not damaging to the first and second structures but are sufficient to form bonds that are strong enough to survive subsequent processing at temperatures higher than that used during the bonding and the bonding interface produced by the annealing is strong enough to be substantially unaffected by processing of the combined structure. Similarly, Claim 48 recites specific annealing temperatures. The passages cited by the Examiner (col. 7, lines 55-65 and col. 12, lines 1-15) do not describe bonding conditions, nor anything to do with a comparison between the bonding conditions and subsequent processing conditions.

Claim 40 recites that the bonding interface produced by the annealing is substantially optically transparent to light emitted by the combined structure. The passage denoted by the Examiner (col. 12, lines 1-15) does not teach qualities of the interface, nor specifically that the interface is optically transparent.

Claims 44 and 45 recite selecting a composition of the bonding layer such that an amorphous layer is deposited on at least one of the first and second structures and that the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material from the amorphous layer, respectively. Similarly, Claims 46 and 47 recite selecting a composition of the bonding layer such that a polycrystalline semiconductor layer is deposited on at least one of the first and second structures and the annealing of the combined structure occurs under conditions sufficient for the bonding layers to recrystallize into a polycrystalline material, respectively.

However, the passages indicated by the Examiner discuss the composition of the substrate on which the layers are disposed rather than the structure of the bonding layers. Nowhere does Malik discuss any low temperature grown deposited structures. Nor do the passages pointed to by the Examiner discuss anything about phase changes or recrystallization during the annealing process. As mentioned above, Malik only teaches that during subsequent processing it is necessary to choose low temperatures so that the porous layer does not change structurally.

Claims 50-51 recite doping the bonding layer. Malik discloses noble gas, hydrogen and nitrogen implantations. However, implantations such as these are not dopants in a semiconductor. Dopants affect the electronic properties of the semiconductor into which they are introduced by giving unbonded electrons to the material or accepting unbonded electrons from the material. Malik does not disclose doping the bonding layer with a dopant such as Si (Claim 51).

Claim 53 recites that the bonding layer is deposited by molecular beam epitaxy (MBE) at a temperature of at most about 100°C. As indicated numerous times, the passage indicated by the Examiner discusses treatment after annealing. This passage (col. 8, lines 1-15) has nothing to do with the growth conditions of the bonding layer. In

particular, nowhere does Malik describe specifically either the type of chamber in which the bonding layer is deposited or the temperature used during growth.

Regarding Claim 82, which recites that the bonding layer is devoid of polymers, ceramics, and metals, again the passage (col. 8, lines 1-15) cited by the Examiner merely discusses the type of material that the non-porous film can be made of, among other irrelevant information. However, nowhere does Malik specifically state that the bonding layer that the bonding layer is devoid of polymers, ceramics, and metals.

Claim 52 recites that the first and second structures are separate structures from each other before the bonding layers are placed in contact and the combined structure is annealed. Thus, the bonding layers cannot be layers 52 and 54 as these layers do not bond the first and second structures together. As is clear from the description of Figs. 3A-3F, specifically col. 8, lines 29-34, the non-porous bonding layers 54 and 55 are placed in contact with support substrates 58 and 59 and these surfaces are bonded together. This is entirely different from placing bonding layers on separate structures such that they contact each other and bonding these structures together.

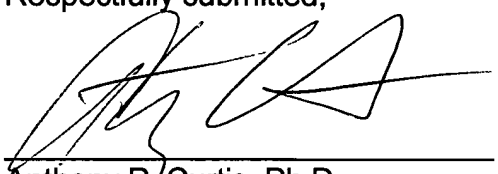
For at least these additional reasons, the dependent claims are independently patentable over Malik.

For at least these reasons, Malik does not anticipate or disclose the arrangements of Claims 101-119. Accordingly, Claims 101-119 are patentable over Malik.

Conclusion

Applicant respectfully submits that all of the pending claims are in condition for allowance. If for any reason the Examiner is unable to allow the application in the next Office Action and believes that a telephone interview would be helpful to resolve any remaining issues, she is respectfully requested to contact the undersigned.

Respectfully submitted,



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